REMARKS

In response to the Office Action, Applicant respectfully requests the Examiner to reconsider the above-captioned application in view of the foregoing amendments and the following comments.

Discussion of Claim Rejections Under 35 U.S.C. §§ 102(e) and 103(a)

In the Office Action, the Examiner rejected Claims 2-7 and 9-11 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,764,590 to Iwamoto (hereinafter "Iwamoto"). The Examiner rejected Claims 1 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Iwamoto in view of U.S. Patent No. 5,537,584 to Miyai, et al (hereinafter "Miyai").

One embodiment of Applicant's invention includes a switch that is used to control the parasitic capacitance of a bus. Claim 1, as amended, recites:

> A memory integrated circuit comprising:
>
> one or more data input/output terminals;
>
> *an input buffer*;
>
> a state decoder for receiving a chip select signal targeted for the memory integrated circuit; and
>
> a parasitic capacitance control bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer, wherein the switch is an integral part of the memory integrated circuit, and wherein the *input buffer* is selectively *electrically* decoupled from *each of* the terminals in response to a change in state in the chip select signal, the switch being operated so as to control the parasitic capacitance of the terminals in response to receiving the chip select signal.

Claims 2, 4, 7-9, and 11 recite similar types of limitations.

Applicant respectfully submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *See* M.P.E.P. § 2131. Furthermore, to establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *See* M.P.E.P §

2143.03. Applicant respectfully submits that the cited references fail to teach or suggest at least one limitation from Claims 1, 2, 4, 7-9 and 11.

Iwamoto describes a selector (904). The selector (904) routes signals from a input buffer to one of two write registers. *See* Iwamoto, col. 11, line 50 - col. 12. line 3. Applicant respectfully submits that there is no teaching or suggestion in Iwamoto that the selector (904) is used to electrically decouple a buffer from each of the contacts of a data bus. The selector (904) merely acts as a router of information. The input selector (904) is merely used to functionally activate a signal to either an input buffer A or an input buffer B. Figure 11 illustrates a specific configuration of an input selector (904). The input selector (904) is comprised of inverters (1101 and 1102). In Iwamoto, the terminals 112 and 113 are always electrically coupled to one of input buffers A or B.

Iwamoto states the following:

> Referring to FIG. 11, input selector 904 includes an inverter 1101 activated in response to mode setting signal B8E, and an inverter 1102 activated in response to mode setting signal /B8E. Logic levels of mode setting signals B8E and /B8E are determined by bonding option as shown in FIG. 5. When x8 configuration mode is set, mode setting signal B8E is set to H level and mode setting signal /B8E is set to the L level. Therefore, the data signal DQi from data input/output terminal 112 is applied to input buffers 905a and 905b, while data signal DQi+1 from data input/output terminal 113 is not applied to input buffer 905b. By contrast, when the x16 configuration mode is set, mode setting signal B8E attains to the L level and the mode setting signal /B8E attains to the H level. Therefore, the data signal DQi from data input/output terminal 112 is applied to input buffer 905a, data signal DQi+1 from data input/output terminal 113 is applied to input buffer 905b, while the data signal DQi from data input/output terminal 112 is not applied to input buffer 905b.

See col. 12, lines 4 -22. Thus, in Iwamoto, input buffer A (905a) or input buffer B (905B) is always electrically connected to one of the input terminal 112 or the input terminal 113. In contrast, in one embodiment of the invention, the input buffer is electrically decoupled to each of the contacts or terminals of a data bus.

Thus, Applicant respectfully submits that since Iwamoto does not teach or suggest each and every element of Claims 2, 7, 9, and 11, these claims are not anticipated and are in condition for allowance.

Furthermore, Applicant respectfully submits that these features are not taught or suggested by Miyai. Miyai was cited by the Examiner in support of the proposition that chip select signals were well known in the art. Applicant respectfully submits that Miyai fails to teach or suggest the use of a chip select signal so as to electrically decouple a portion of bus. In the Office Action, the Examiner stated that in independent Claims 1 and 8, the control of the parasitic capacitance is independent of the chip select signal. Applicant respectfully submits that these claims have been amended to clarify this issue.

Since Iwamoto and Miyai fails to teach or suggest at least the above limitation in isolation or in combination, Applicant respectfully submits that independent Claims 2, 4, 7-9, and 11 are in condition for allowance. Furthermore, since Claims 3 and 5 each depend on one of Claims 2, 4, and 9, Applicant respectfully submits that these claims are allowable for the reasons previously discussed.

Summary

Applicant has endeavored to address all of the Examiner's concerns as expressed in the outstanding Office Action. Accordingly, amendments to the claims for patentability purposes, the reasons therefore, and arguments in support of the patentability of the pending claim set are presented above. Any claim amendments which are not specifically discussed in the above remarks are not made for patentability purposes, and the claims would satisfy the statutory requirements for patentability without the entry of such amendments. In addition, such amendments do not narrow the scope of the claims. Rather, these amendments have only been made to increase claim readability, to improve grammar, and to reduce the time and effort required of those in the art to clearly understand the scope of the claim language. In light of the above amendments and remarks, reconsideration and withdrawal of the outstanding rejections is specifically requested. If the Examiner has any questions which may be answered by telephone, he is invited to call the undersigned directly.

Respectfully submitted,

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